Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BAL/COMP 1**
2. **– INPUT**
3. **+ INPUT**
4. **V –**
5. **BAL/COMP 3**
6. **OUTPUT**
7. **V +**
8. **COMP 2**

**3**

**4**

**5**

**2 1 8 7**

**6**

**.078”**

**.060”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .060” X .078” DATE: 2/23/16**

**MFG: LINEAR TECH THICKNESS .025” P/N: LM118**

**DG 10.1.2**

#### Rev B, 7/19/02